

REMARKS/ARGUMENTS

In this amendment, no claims are amended, canceled, or added. Thus, claims 1-22 remain pending.

Rejection under 35 U.S.C. §102(b) and 103(a), Rinaldi

Claims 1-2, 5-8, 11-12 and 15-22 were rejected under 35 U.S.C. 102(b) as being anticipate by Rinaldi et al (US Patent No. 6,327,002 B1). Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rinaldi et al. Claims 3-4 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rinaldi et al in view of the admitted prior art (Figs. 1A & 1B, and page 2, [0005]-[0006]).

Claims 1-10, 17-19

Claim 1 is allowable as Rinaldi does not teach or suggest each and every element of claim 1. For example, claim 1 recites:

pixel pipeline circuit configured to provide a pixel stream comprising digital pixel values;
an encoder coupled to an output of the pixel pipeline circuit and configured to convert the pixel stream to digital sample values for a target analog signal representing the pixel stream in the target format, thereby generating a base data stream at a base sampling rate;
a supersampling circuit coupled to an output of the encoder and configured to generate a supersampled data stream at a supersampling rate from the base data stream, the supersampling rate being higher than the base sampling rate; and
a digital to analog converter coupled to an output of the supersampling circuit and configured to convert the supersampled data stream to an analog output signal.

A/D module receives analog signal not digital values, and switching matrix (i.e. multiplexers) passes signals without any conversion of the signal.

In claim 1, the data appears in three different formats. Initially, the data is in "*a pixel stream comprising digital pixel values*" (c.g., as RGB color components). See *specification*, paragraph 28. Secondly, the encoder converts "*the pixel stream to digital sample values for a target analog signal.*" *Id.*, paragraph 29. For example, where the target analog

stream is NTSC, the digital samples would provide appropriate amplitude and/or phase values at 54 million samples per second. *Id.*, paragraph 30. Note that the supersampled data stream is still digital samples of the target analog signal, albeit at a higher sampling rate. *Id.*, paragraph 31. To produce the target analog signal, the digital samples are converted to "an analog output signal" via the digital to analog converter. *Id.*, paragraph 34. Thus, the digital samples only need to be converted to analog format to obtain the target analog signal.

At page 3 in the Response to Arguments, the present Office Action asserts that the A/D conversion module 54 of Rinaldi corresponds to the encoder of claim 1. As suggested by its name, the A/D conversion module 54 receives analog signals. *See Rinaldi*, page 2 and col. 3 lines 42-45. In contrast, claim 1 recites that the encoder receives digital pixel values. Thus, the A/D conversion module 54 cannot correspond to the encoder of claim 1. It is the video encoder 22 that can receive digital pixel values from the graphics controller 24 and sends digital sample values to the DAC 23. *Id.*, FIGS. 1-1 and col. 3 lines 18-25.

Note that page 5 of the Office Action is inconsistent with the Response to Arguments section as outlined above. At page 5, the Office Action asserts that the input switching matrix 68 is the encoder of claim 1. Presumably, this is an artifact of the previous Office Action. In any event, the matrix 68 is simply multiplexors that determine whether processed or non-processed digital sample values are sent to the upsampling module 70. *Id.*, col. 3 lines 63-66. Multiplexors are signal selection circuits, where based on a setting only the selected circuits are transmitted. A multiplexer does not convert a format of a signal it receives, but simply transfers the selected signal without any change or conversion of the signal. Thus, the switching matrix 68 also cannot be the encoder as recited in claim 1.

Upsampling module 70 has rate equal to target signal, not higher

Additionally, at page 3, the Office Action states that the upsampling module 70 can upsample the digital signal to a higher sampling rate than the signal that is input into it, and thus it teaches a supersampling circuit that generates data at a supersampling rate higher than the base sampling rate of the output target analog signal, as recited in claim 1. However, the upsampling circuit 70 "changes the sampling frequency of the signals to match the desired output

sampling frequencies," and not to be higher than the output sampling frequencies. *Id.*, col. 4 lines 6-7. The present invention advantageously uses a sampling rate higher than that of the target output signal in order to suppress echoes. *See specification*, FIGS. 4C and 4D and paragraph 39.

For at least these reasons, claim 1 is allowable over Rinaldi. As claim 1 is allowable, dependent claims 2-10 are also allowable for at least the same rationale.

Applicants submit that independent claim 17, and its dependent claims 18-19, are allowable for at least the same reasons as claim 1.

Claims 11-16, 20-22

Claim 11 is allowable as Rinaldi does not teach or suggest each and every element of claim 11. For example, claim 11 recites:

a supersampling circuit coupled to an output of the pixel pipeline circuit and configured to generate a supersampled pixel stream comprising a second number of digital pixel values per line, the second number being greater than the first number, at a supersampling rate higher than the base pixel rate;
an encoder coupled to an output of the supersampling circuit and configured to convert the supersampled pixel stream to digital sample values for a target analog signal representing the supersampled pixel stream in the target format, thereby generating a supersampled data stream at an enhanced sampling rate.

At page 4, the Office Action concludes that the switching matrix 72 converts a "supersampled pixel stream to digital sample values for a target analog signal." The only rationale presented is that it is clear from the passage: "[b]ased on output commands, the output switching matrix 72 provides the output of the up sampling module 70, the YUV video data 80, or a combination thereof to the digital-to-analog conversion module 23." *See Rinaldi*, col. 4 lines 11-14. This sentence simply states that the switching matrix is a signal selection circuit made up of multiplexors just like switching matrix 68, as described above. The desired output is chosen by selecting which of different inputs to allow to pass through to an output. As is well known in the art, a multiplexor does not convert an input signal, but simply passes through the selected signal unchanged. Thus, matrix 72 does not correspond to an encoder "to convert the

supersampled pixel stream to digital sample values for a target analog signal,” as recited in claim 1. Accordingly, Rinaldi does not teach or suggest this limitation.

For at least these reasons, claim 11 is allowable over Rinaldi. As claim 11 is allowable, dependent claims 12-16 are also allowable for at least the same rationale.

Applicants submit that independent claim 20, and its dependent claims 21-22, are allowable for at least the same reasons as claim 11.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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